## 1. GENERAL DESCRIPTION

UST2019 IC is a powerful 4-bit micro-controller based sound processor. They are embedded EPROM architecture, and the OTP (One Time Programmable) ICs. There are 4 channels that are configured as speech or midi, and all of them can be autoplayed back simultaneously. By using the high fidelity ADPCM speech synthesis algorithm, it can produce outstanding quality voices. Wide range sampling rate up to 44.1kHz and different volume level are supported. It is also equipped two kinds of audio outputs with fine resolution,including a current D/A converter and a PWM direct-driver.The RISC MCU architecture is very easy to to program and control, various applications can be easily implemented.There are 48 instructions, and most of them are executed in single cycle.Furthermore,in addition to the HALT mode (sleep mode), it offers the SLOW mode to minimize power dissipation.

2. FEATURES

- Wide operating voltage range: 2.0V to 5.5V.

- 4-bit RISC type micro-controller with 48 instructions.

- 224x4-bit RAM maximum, divided into 4 pages.

- 1MHz or 2MHz instruction frequency.

- SLOW mode to operate at low power consumption. *(Not suggest using in Timer/Clock application.)*

- HALT mode to save power, less than 1uA@3V standby current.

- Precisely embedded oscillator with build-in resistor (+/- 1%). External resistor to adjust system frequency is optional.

- Low voltage reset (LVR=1.8V), watch-dog reset and I/O port reset are all supported to protect the system.

- One interrupt entrance with an independent stack, multiple interrupt sources.

- Maximum 24 flexible I/Os maximum with optional function: input, output, large current output, IO, floating-type reset, pull-high reset, IR carrier output and large current IR carrier output. For the output port, users can select the normal Drive current output or large Sink current output to directly drive high brightness LED.

- Support Open-Drain (OD) bi-direction IO.

- Infrared output: optional IR carrier frequency and optional data high/low IR output supported.

- Maximum of 4 channels can play simultaneously; each channel can be arbitrarily assigned as speech or Midi channel based on the product spec.

- New high fidelity ADPCM speech synthesis algorithm.

- 3 kinds of 256 points, ADSR and Full-Wave instrument waveform provide outstanding midi quality for MIDI.

- 256 steps envelope control for Midi.

- High quality 9-bit PWM to directly drive speaker, or 10-bit D/A converter audio output to amplify the volume by external audio amplifier for multi-channel MIDI especially.

- Support large PWM current output.

- 16 steps volume control for audio output.

- Quick-IO control supported.

- A unique fast writing mode is provided to speed up OTP writing time.

- A special ICP *(In Circuit Programming)* writing function is supported for user to fabricate PCBA in advance.

- Programmable code protection is provided. *(When the Security-Bit is burnt down, data can't be read.)*

- Various shipping type for different application requirement.
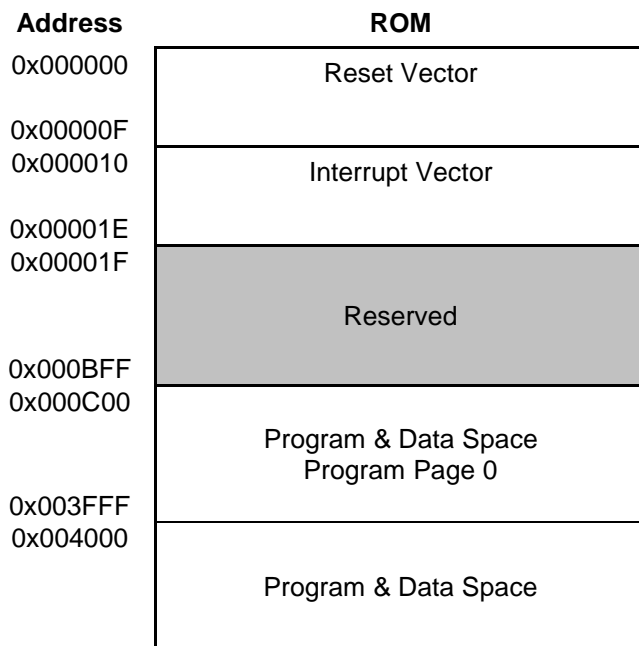
3. BLOCK DIAGRAM
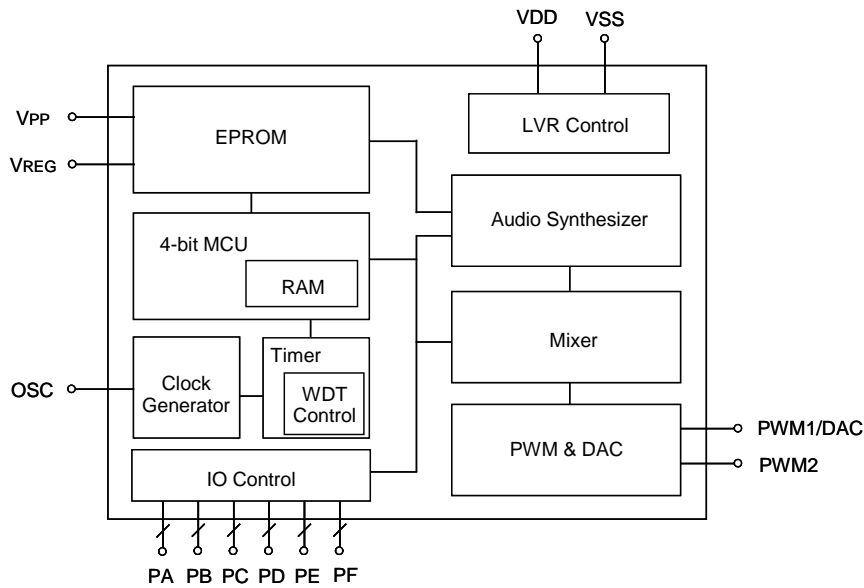
4. PIN DESCRIPTION

Pin Number	NAME	Description
1	PWM1	PWM1 output or DAC output.
2	PWM2	PWM2 output, or select programming mode.
3	VDD1	Positive power.
4	PB3	I/O
5	PB2	I/O
6	VPP	Positive high power for programming.
7	NC	NC
8	NC	NC .
9	NC	NC .
10	NC	NC
11	VDD2	Positive power.
12	VDD3	Positive power.
13	PA0	I/O
14	PA1	I/O
15	PA3	I/O
16	PC0	I/O
17	GND4	Negative power.
18	GND3	Negative power.
19	GND2	Negative power.
20	GND1	Negative power.

5. MEMORY ORGANIZATION

There are maximum 1728K words EPROM, 224 nibbles of RAM and 19 nibbles of dedicated system control register. The registers are divided into 11 nibbles of system registers and 8 nibbles of memory registers. Besides, there are several registers without address allocation, and they can only be accessed by the special instructions. One of the registers is RAM page register (PG), and the others are audio control registers.

5.1 ROM

A large program/data/voice single ROM is provided, and its structure is shown below. The reserved region contains system information and can't be utilized by users. The program page is limited by the unconditional branch instruction: JMP and CALL. Because it can only handle 14-bit length address of ROM, the program page size is 16K words.

Address	ROM
0x000000	Reset Vector
0x00000F	
0x000010	Interrupt Vector
0x00001E	
0x00001F	Reserved
0x000BFF	
0x000C00	Program & Data Space Program Page 0
0x003FFF	
0x004000	Program & Data Space

5.2 RAM

Each page of RAM contains 56 nibbles, and NY5P serial provides 224 nibbles of 4 pages. The page number (PG) register of RAM defined by the MPG instruction, and its initial value is 0. Because the memory space is shared with the memory registers (address=0x00~0x07), the address for RAM is 0x08~0x3F.

In addition to the immediate addressing mode, the indexed addressing mode is also supported. The page and address of the indexed RAM should be stored into RPT1 and RPT0 first, and users can read from or write in the XMD memory register to realize the indexed ROM access.

6. IO PORTS

There are most 6 I/O ports, designated as PAx through PFx, and x=0~3. All the I/O ports can be configured as input, output, or IO port (bi-direction). For the input port, we provide an internal pull-high register option for convenience. For the output port, users can also option its initial value as low or high according to your application circuit. Besides, users can also enable the large current option for each output port to get a larger sink current. The bi-direction IO port can be an input or output by its register value, and users can option the bi-direction IO with a pull-high resister or without a pull-high resister (Open-Drain). When the register equals 0, it is an output and can only output zero. When the register equals 1, it is a weak pull-high or floating (Open-Drain) so that it also can be considered as an input port with/without a pull-high resistor. Users also can enable the large sink current option of an IO port.

The PX0 port means the PA0, PB0, PC0, PD0, PE0 or PF0 port can also be optioned as an external reset pin or an infrared (IR) output pin. A reset port can possess a pull-high resister or not, and an IR port can be initial low or high and also large sink current or not.

The pull-high resister of all the I/O ports has two kinds of option: weak and strong. The weak one is about 850KΩ @3V for normal application and the strong one is about 480KΩ @3V usually for key matrix function. When users configure the weak or strong pull-high resister, the pull-high resisters of all I/O ports are set as the option value.

7. AUDIO SYNTHESIZER

There are 1-ch voice and 2-ch or 4-ch speech/Midi, and all modes are auto-played back by hardware. Different channel mode possesses different hardware structure. It provides a hardware mixer to mix the channel data. The mixer contains a mixer control register MIX. 1-ch ~ 4-ch voice and/or Midi are all configurable by programming the MIX Two audio output stages: DAC and PWM are supported.

7.1 Voice

A voice channel includes a PFLG, a VPR, a voice decoder, a QIO control code generator and an 8-bit sample rate timer (TM) whose timer clock source (TCS) is fixed to 1MHz. It supports PCM and encoded ADPCM speech data.

7.2 Midi

A Midi channel includes a PFLG, a VPR, a TM, an ENV, a timbre skipper and a multiplier, which multiplies the Midi data and the envelope value held by the ENV. The timbre skipper is used to fulfill the higher octave pitch playing. The hardware multiplier is dedicated to the Midi channel, and users can't operate it by any instruction.

7.3 Audio Output

By setting the AUD register, PWM or DAC can be easily chosen as the audio output stage. Besides, it provides a pad detecting mechanism. The pad detecting mechanism detects the PWM2 pad during the reset initialization period, and sets the initial value of the audio output register as PWM if the PWM2 connection is floating, or sets the initial value of the audio output register as DAC if the PWM2 connection is high. In conclusion, connect the speaker to PWM1 and PWM2 only if using PWM, otherwise connect PWM2 to VDD if using DAC. Since the mechanism sets only the initial value of AUD, don't change the value of the AUD register if the pad detecting mechanism is adopted.

PWM Output Connection   *DAC Output Connection*   *PWM/DAC Connection Together*
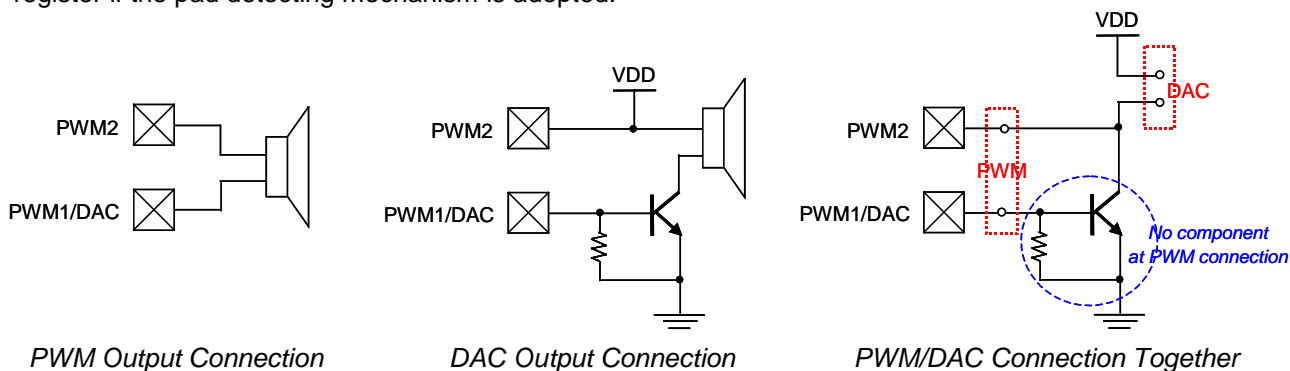
When using the PWM output, we provide an option of normal PWM current or large PWM current for different customer demand. The large PWM consumes more current and makes sound louder.

7.4 Volume Control

Both PWM and DAC support 16 steps hardware volume control by the VOL register.

8. ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Rating

Symbol	Parameter	Rated Value	Unit
Vdd - Vss	Supply voltage	-0.5 ~ +6.0	V
Vin	Input voltage	Vss–0.3V ~ Vdd+0.3	V
Top	Operating Temperature	0 ~ +70	°C
Tst	Storage Temperature	-25 ~ +85	°C

8.2 DC Characteristics

Symbol	Parameter		V_{DD}	Min.	Typ.	Max.	Unit	Condition
V_{DD}	Operating voltage			2.0	3	5.5	V	1MHz & 2MHz
I_{sb}	Supply current	Halt mode	3			1	uA	Sleep, no loading
			4.5			1		
I_{sl}		Slow mode	3		150		uA	1ms interrupt, no load
			4.5		350			
I_{op}		Operating mode	3		2		mA	1MHz, no loading
			4.5		2.4			
			3		2.5		mA	2MHz, no loading
			4.5		2.8			
I_{il}	Input current (Internal pull-high)	Weak (850k ohms)	3		-3.5		uA	V_{il}=0v
			4.5		-10			
		Strong (480k ohms)	3		-7		uA	
			4.5		-20			
I_{oh}	Output high current		3		-10		mA	V_{oh}=1.0V
			4.5		-22			V_{oh}=2.2V
I_{ol}	Output low current (Normal current)		3		10		mA	V_{ol}=2.0V
			4.5		20			V_{ol}=2.5V
	Output low current (Large current)		3		20		mA	V_{ol}=2.0V
			4.5		40			V_{ol}=2.5V
I_{PWM}	PWM output current (Normal)		3		60		mA	Load=8 ohms
			4.5		100			
	PWM output current (Large)		3		70		mA	Load=8 ohms
			4.5		117			
I_{DAC}	DAC output current		3		-0.36 ~ -4.20		mA	Half scale
			4.5		-0.47 ~ -4.85			
$\Delta F/F$	Frequency deviation by voltage drop		3		1.5		%	$\dfrac{Fosc(3.0v)-Fosc(2.4v)}{Fosc(3v)}$
			4.5		0.5			$\dfrac{Fosc(4.5v)-Fosc(3.0v)}{Fosc(4.5v)}$
$\Delta F/F$	Frequency lot deviation		3	-1		1	%	$\dfrac{Fmax(3.0v)-Fmin(3.0v)}{Fmax(3.0v)}$
Fosc	Oscillation Frequency		-	0.90	1	1.05	MHz	V_{DD}=2.0~5.5V
				1.80	2	2.10		

8.3 Voltage vs. Frequency

Voltage vs Frequency (6.0KHz@3V)

Voltage vs Freq. Deviation (6.0KHz@3V)
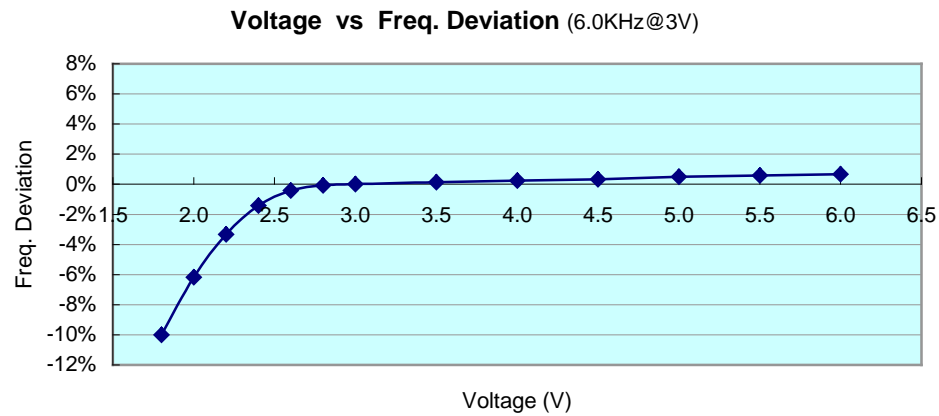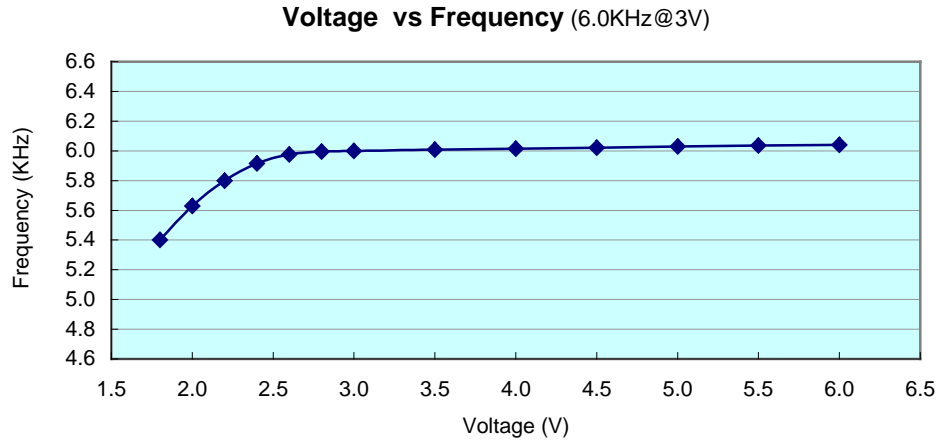
8.4 System Frequency v.s. External Rosc

System Frequency vs External Rosc (1M & 2MHz)
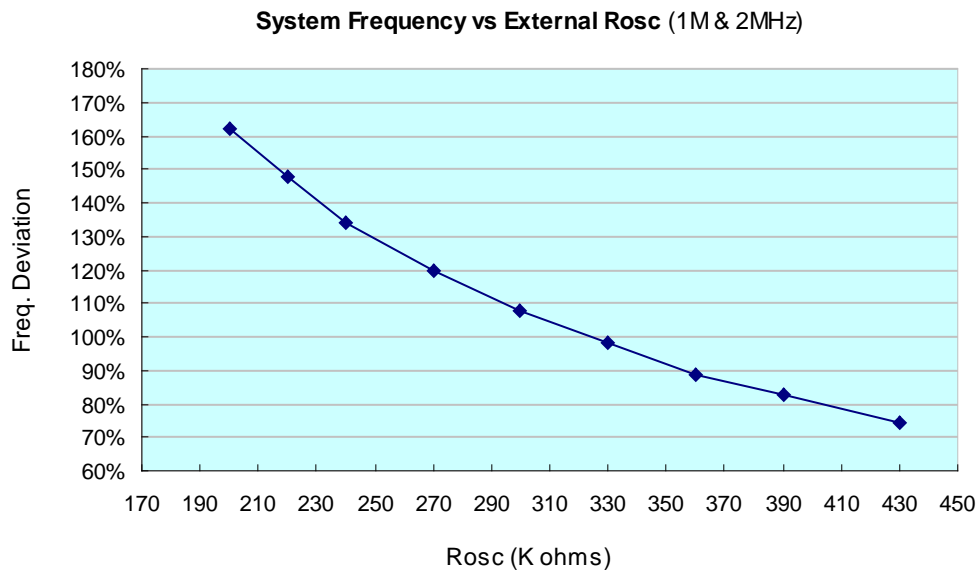
9. APPLICATION

(1) INT-R, PWM *(OSC/PE3 is optioned as PE3 pad)*
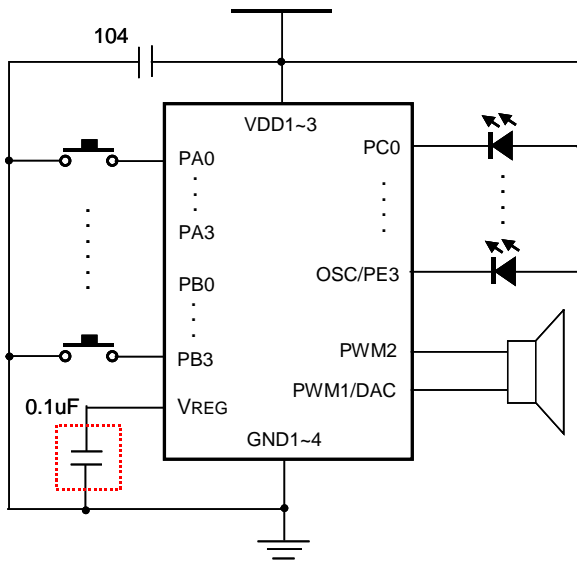
(2) EXT-R, DAC *(OSC/PE3 is optioned as OSC pad)*
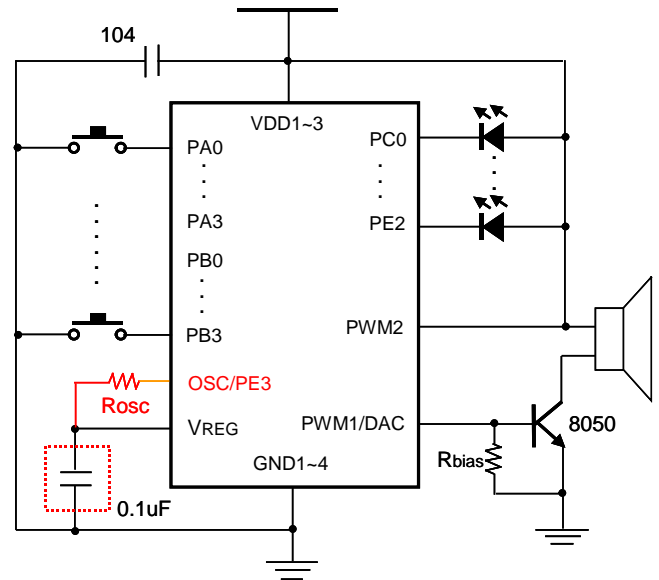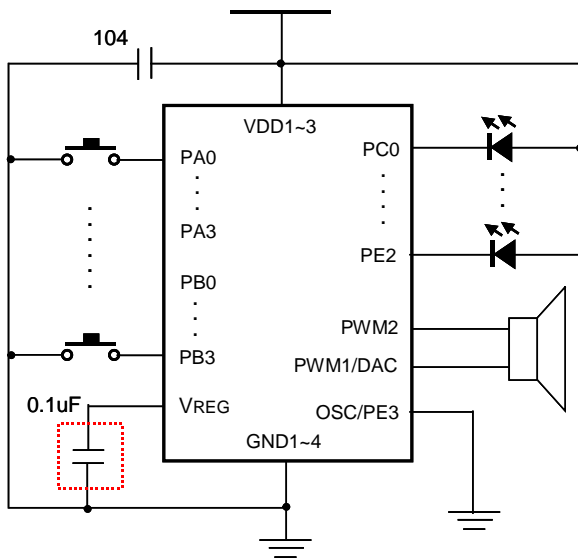
Note: While using external OSC, the OSC pad must be connected to V_{REG} rather than VDD.

(3) INT-R, PWM *(OSC/PE3 is optioned as OSC pad)*

Note: At high voltage of 4.5V or higher voltage, V_{REG} maybe need to connect to GND with a 0.1uF cap for less power noise. At 3V, V_{REG} don't need to connect any capacitor and can be kept this pad floating to save a capacitor.

UST2019

10. PACKAGE PIN ASSIGNMENT

20 Pin SSOP

标注 \ 尺寸	最小(mm)	最大(mm)	标注 \ 尺寸	最小(mm)	最大(mm)
A	7.15	7.25	C3	0.152	
A1	0.30TYP		C4	0.172	
A2	0.65TYP		H	0.05	0.25
A3	0.525TYP		θ	12° TYP4	
B	5.25	5.35	θ1	12° TYP4	
B1	7.65	7.95	θ2	10° TYP	
B2	0.60	0.80	θ3	0° ~ 8°	
C	1.45	1.55	R	0.20TYP	
C1	1.65	1.85	R1	0.15TYP	
C2	0.674				